1376.733US1

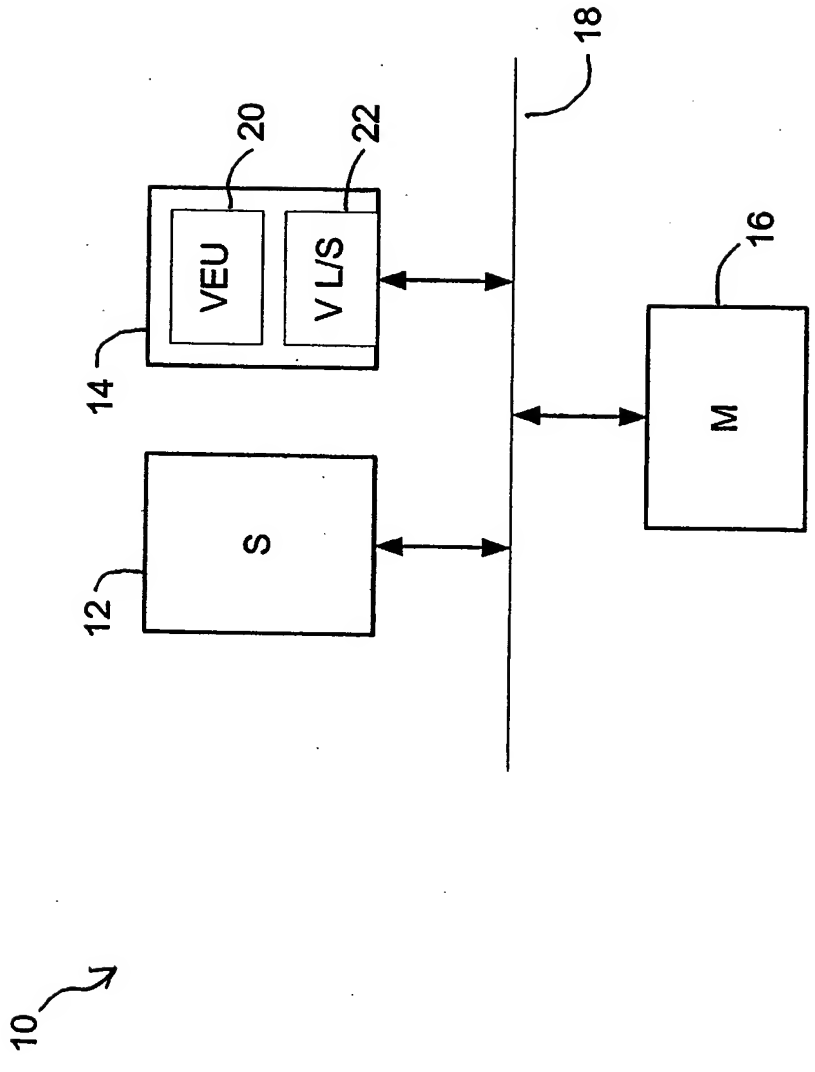


FIG. 1A

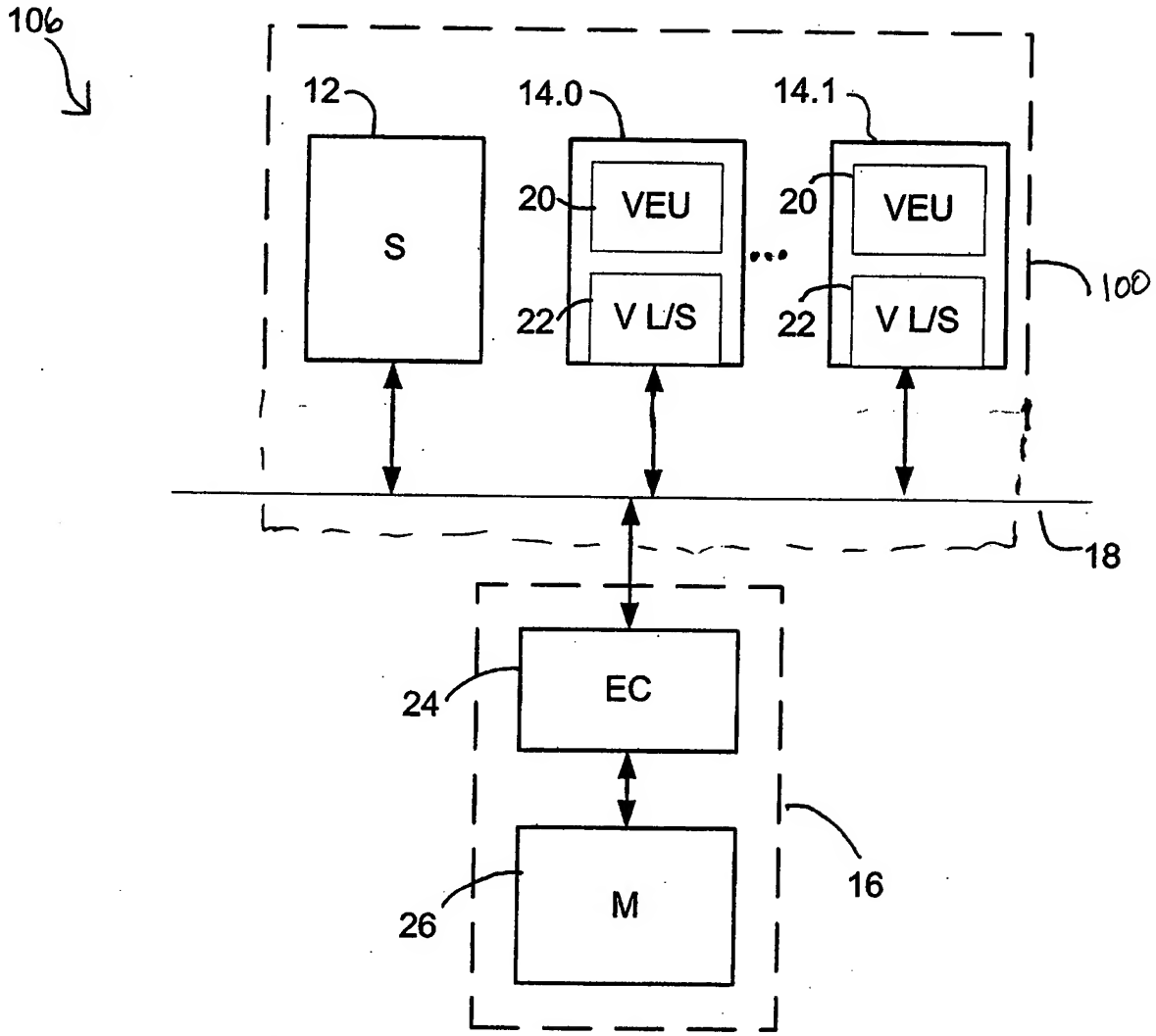
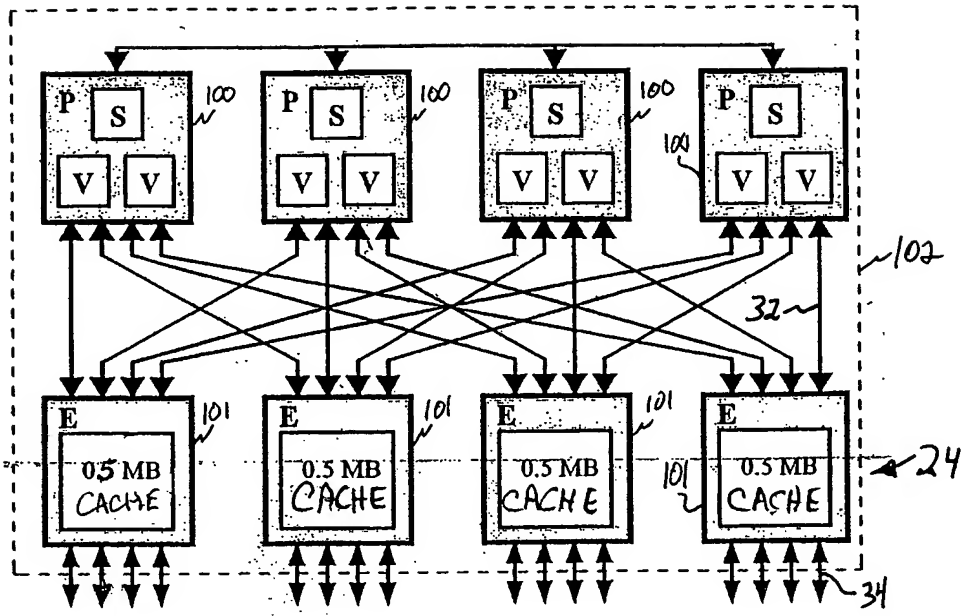


FIG. 1B

FIG. 1C



To local memory and network

FIG 1D

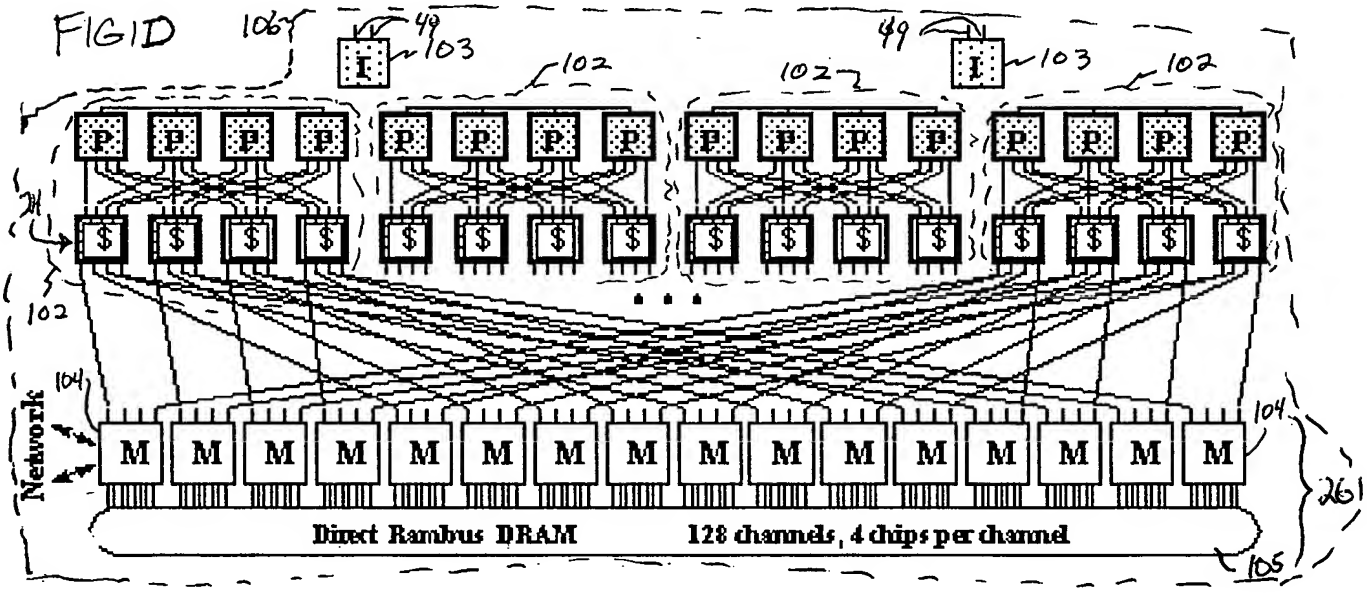
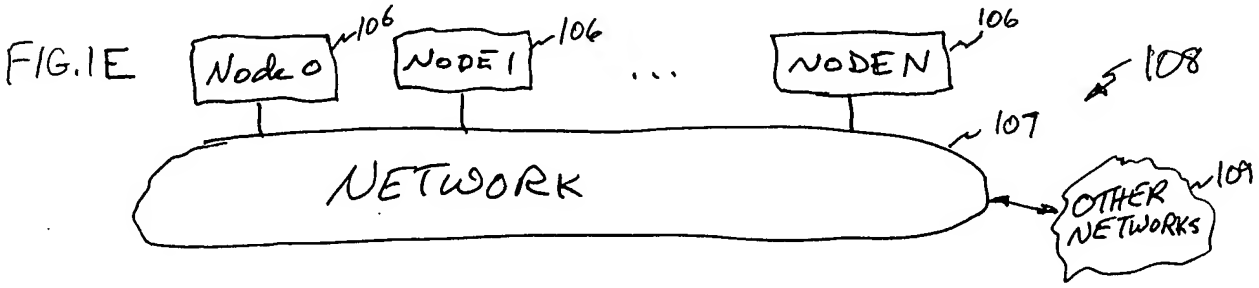


FIG. 1E



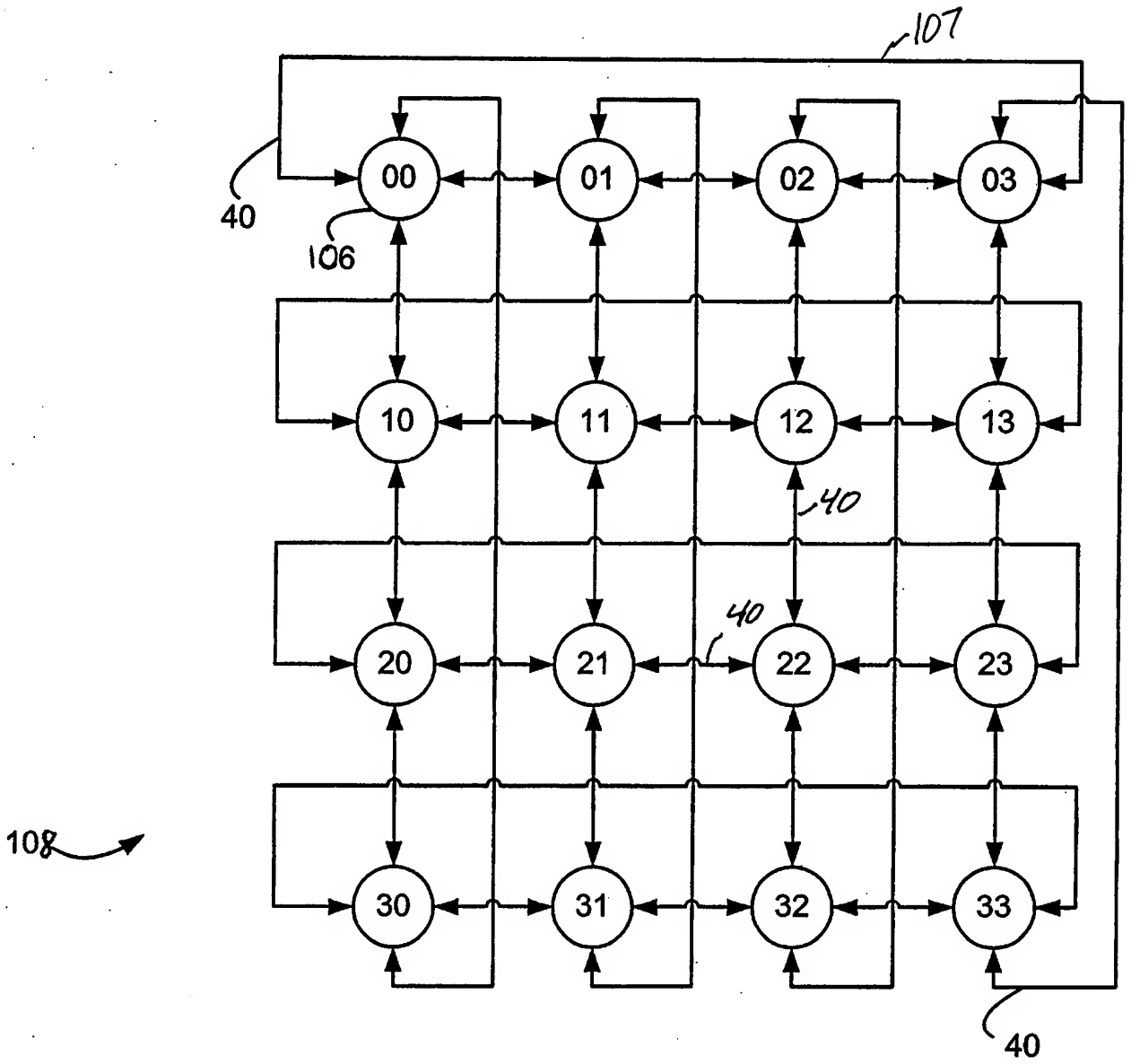


FIG. 1F

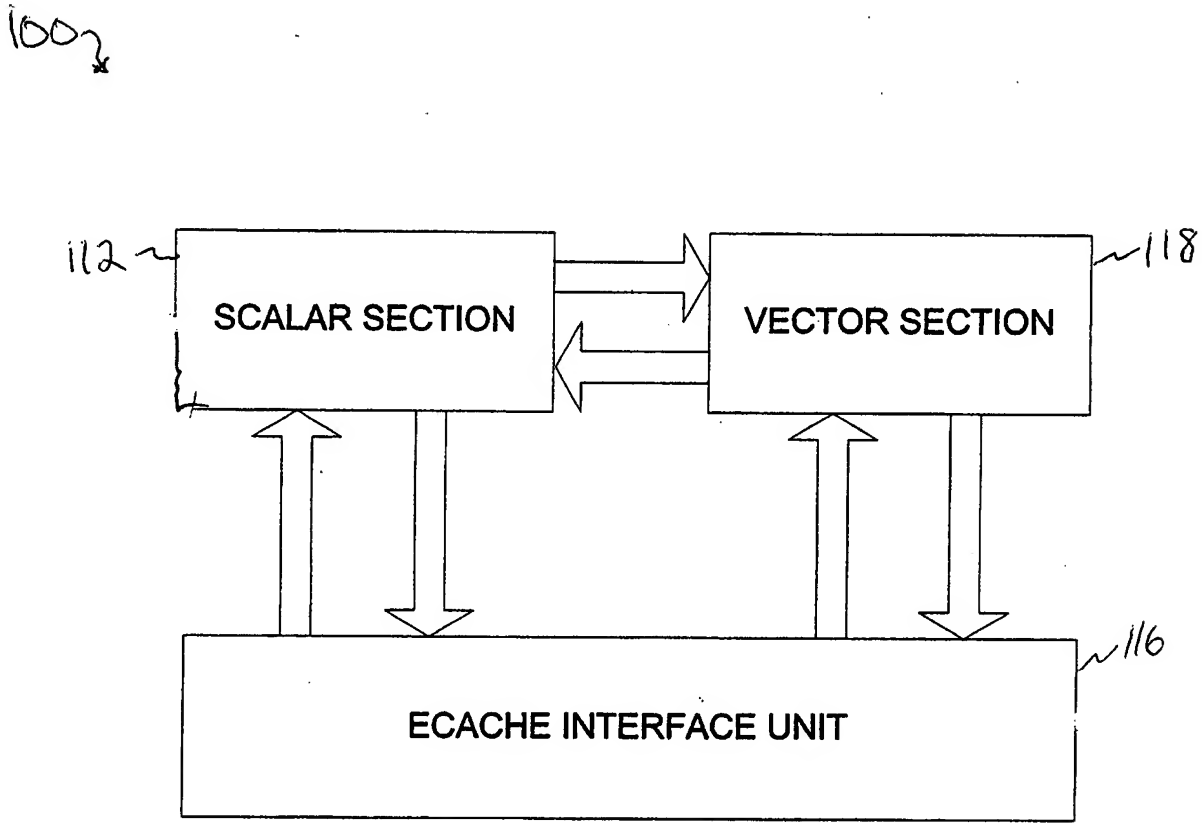

100
112
SCALAR SECTION
VECTOR SECTION
118
116
ECACHE INTERFACE UNIT

FIG. 1G

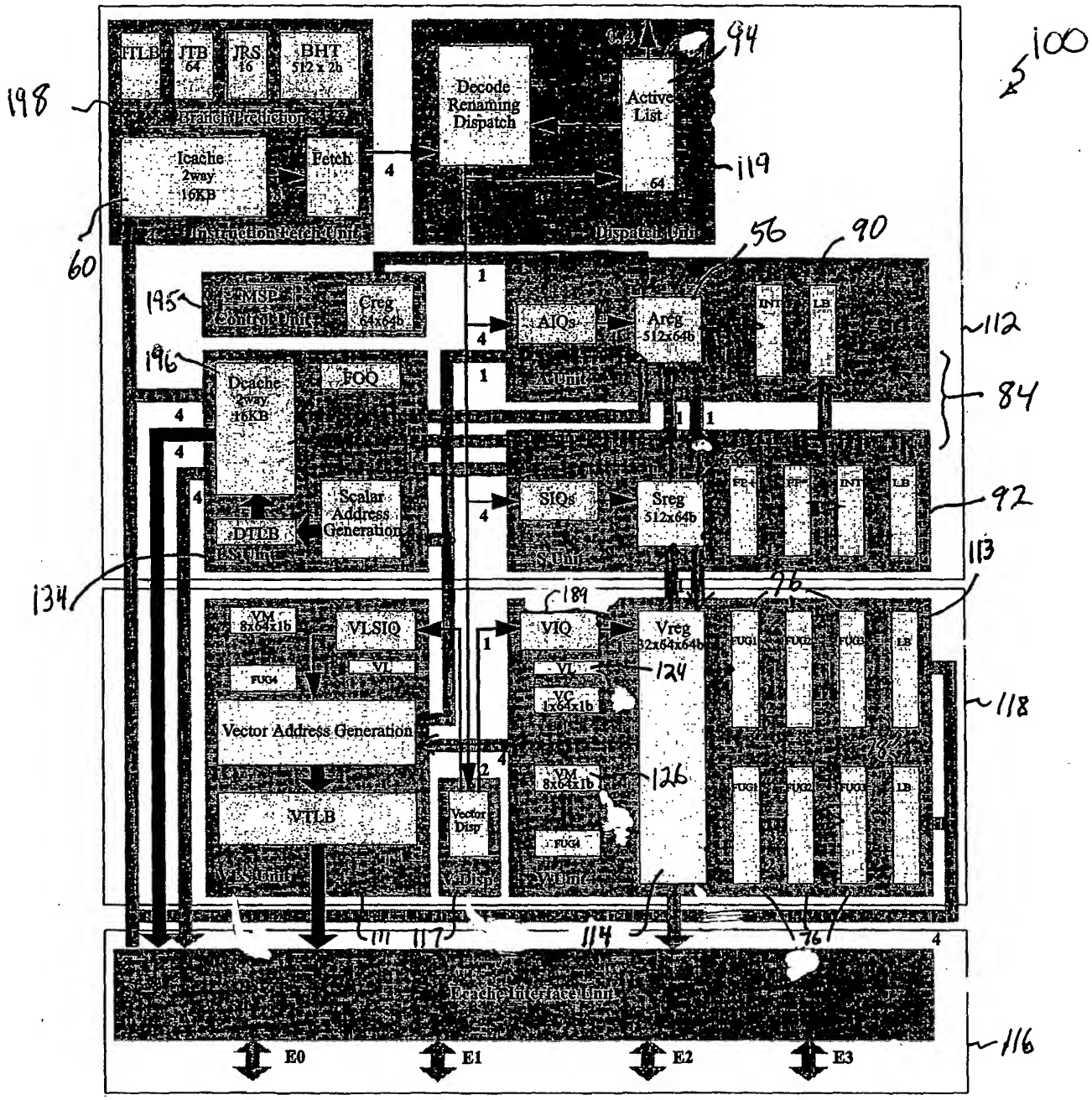

100
198
ITLB
ITB 64
JRS 16
BHT 512 x 2b
Branch Prediction
Icache 2way 16KB
Fetch
Instruction Fetch Unit
60
Decode Renaming Dispatch
Active List
64
94
119
Dispatch Unit
56
90
195
MSP Control Unit
Creg 64x64b
AIQs
Areg 512x64b
A Unit
INT
LB
112
196
Dcache 2way 16KB
FOQ
84
Scalar Address Generation
DTLB
LS Unit
SIQs
Sreg 512x64b
S Unit
FP
INT
LB
92
134
113
189
76
VM 8x64x1b
VLSIQ
VL
FUG4
VIQ
Vreg 32x64x64b
FUG1
FUG2
FUG3
LB
124
VC 1x64x1b
118
Vector Address Generation
VM 8x64x1b
126
VTLB
Vector Disp
VLS Unit
VDisp
VI Unit
111
117
114
76
4
Dcache Interface Unit
116
E0
E1
E2
E3

FIG. 1H

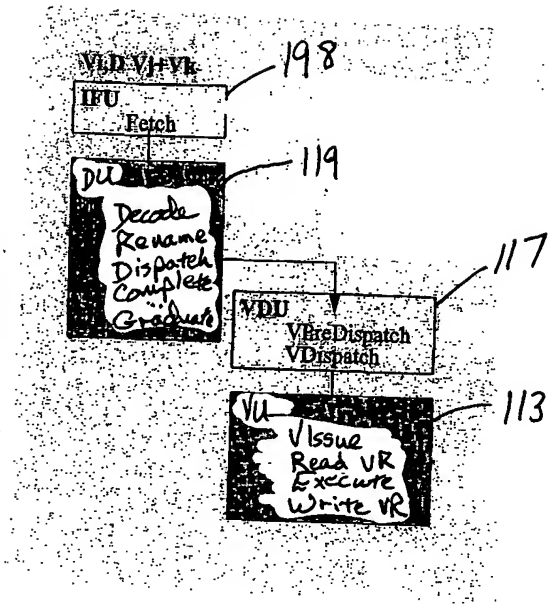

VLD VJ+Vk
198
IFU
Fetch
119
DU
Decode
Rename
Dispatch
Complete
Graduate
117
VDU
VPreDispatch
VDispatch
113
VU
VIssue
Read VR
Execute
Write VR

Fig. 1I

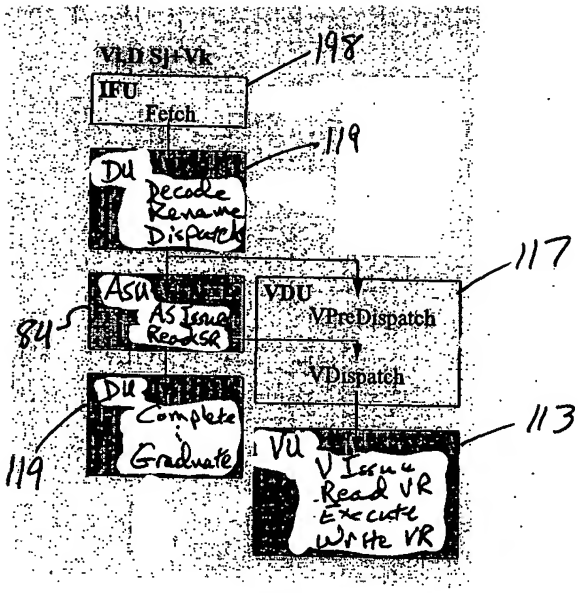

VLD SJ+Vk
198
IFU
Fetch
119
DU
Decode
Rename
Dispatch
117
ASU
AS Issue
Read SR
84
VDU
VPreDispatch
VDispatch
DU
Complete
Graduate
119
113
VU
VIssue
Read VR
Execute
Write VR

Fig. 1J

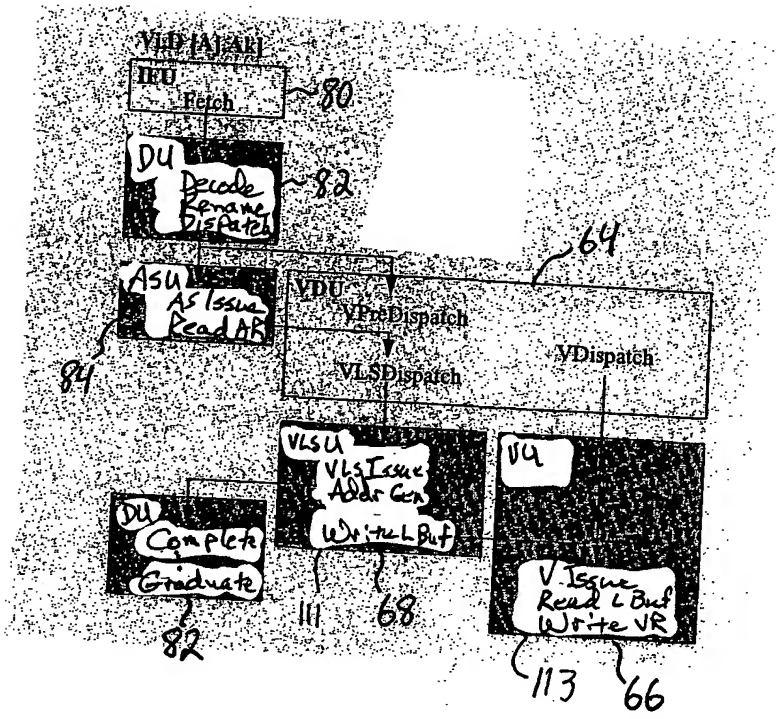
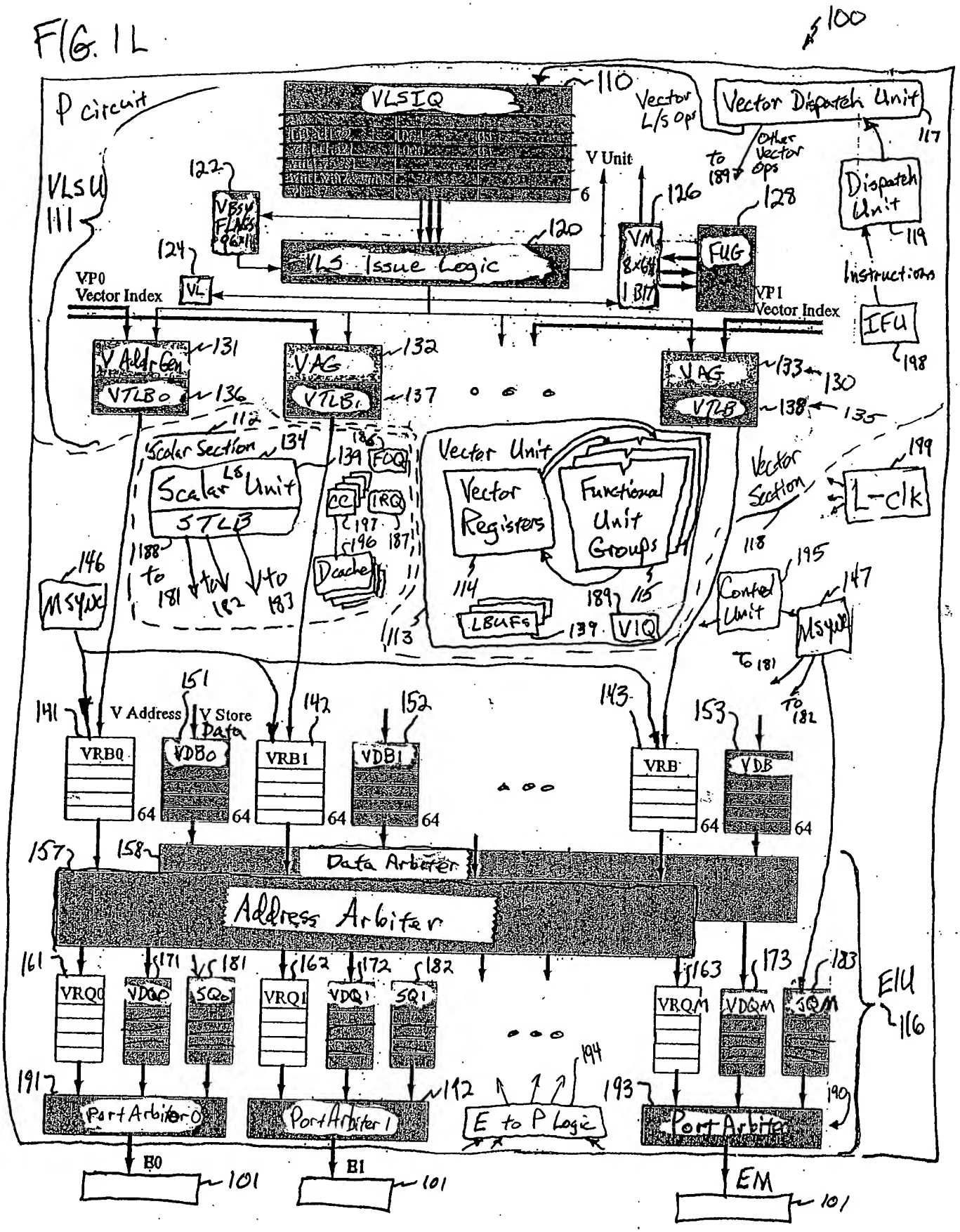

VLIP [A] [AR]
IFU
Fetch
80
DU
Decode
Rename
Dispatch
82
ASU
AS Issue
Read AR
84
VDU
64
VPreDispatch
VLSDispatch
VDispatch
VLSU
VLS Issue
Addr Gen
Write L Buf
VU
V Issue
Read L Buf
Write VR
DU
Complete
Graduate
82
111
68
113
66

FIG. 1K

FIG. 1L


100
P circuit
VLSIQ
110
Vector L/S ops
Vector Dispatch Unit
117
to 189
Other Vector ops
V Unit
6
VLSU 111
122
VBSY FLAGS 963
120
VLS Issue Logic
124
VL
126
VM 8x64 1 BIT
128
FUG
Dispatch Unit
119
Instructions
IFU
198
VP0 Vector Index
VP1 Vector Index
VAddrGen
131
VTLB0
136
VAG
132
VTLB1
137
VAG
133
130
VTLB
138
135
112
Scalar Section
134
Scalar Unit
ST LB
139
FOQ
CC
IRQ
197
196
187
186
Dcache
188
to 181
to 182
to 183
Vector Unit
Vector Registers
Functional Unit Groups
114
115
189
LBUFs
139
VIQ
113
Vector Section
118
199
L-clk
Control Unit
195
147
MSYNC
146
MSYNC
to 181
to 182
141
V Address
151
V Store Data
142
152
143
153
VRB0
VDB0
VRB1
VDB1
VRB
VDB
64
157
158
Data Arbiter
Address Arbiter
161
171
181
162
172
182
163
173
183
VRQ0
VDQ0
SQ0
VRQ1
VDQ1
SQ1
VRQM
VDQM
SQM
EIU
116
191
Port Arbiter 0
192
Port Arbiter 1
194
E to P Logic
193
Port Arbiter
190
B0
101
B1
101
EM
101

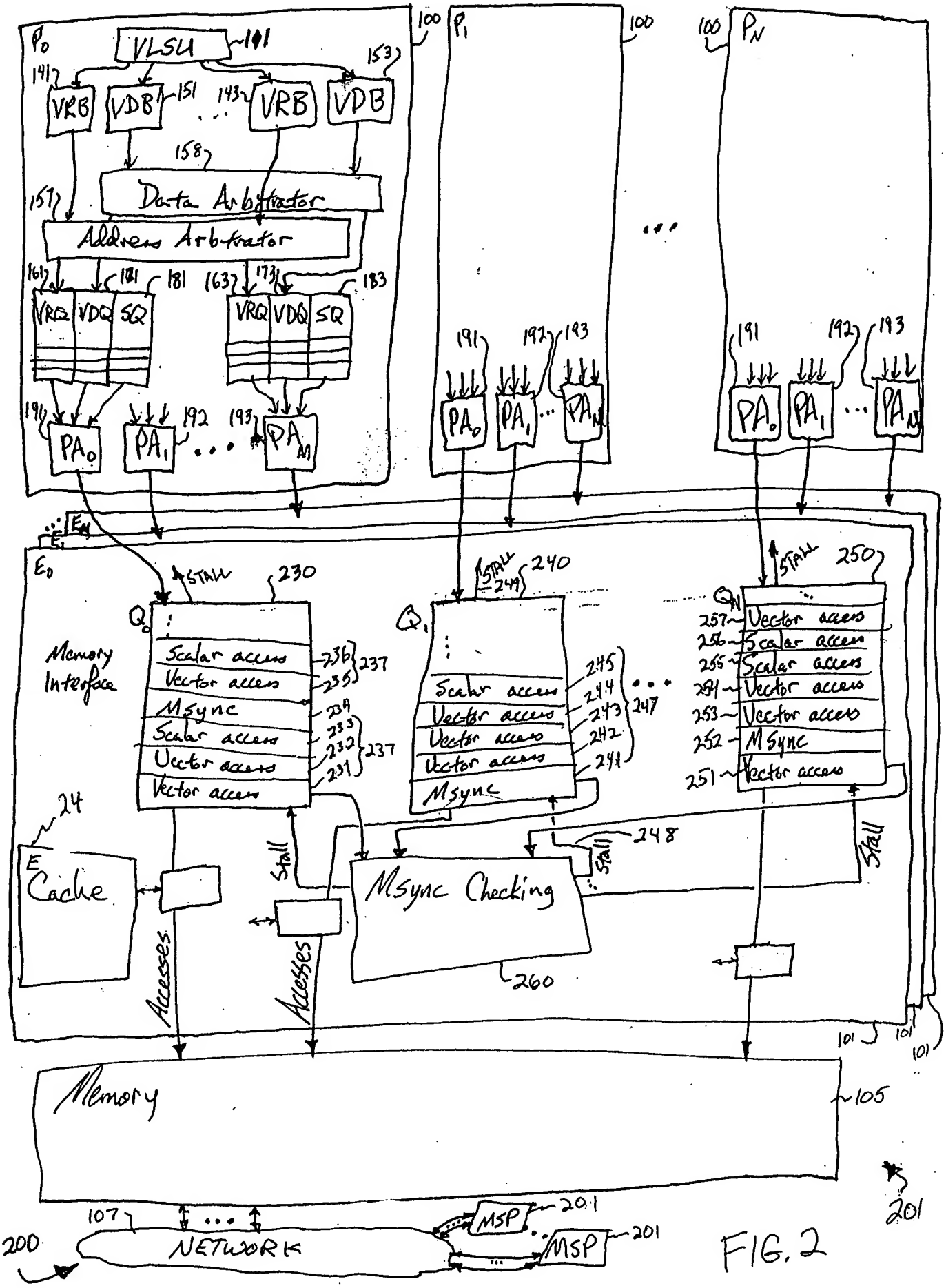

P0
VLSU
101
VRB
VDB
VRB
VDB
Data Arbitrator
Address Arbitrator
VRQ
VDQ
SQ
PA0
PA1
PAM
P1
PN
E0
Stall
Q0
Scalar access
Vector access
Msync
Scalar access
Vector access
Vector access
Q1
Scalar access
Vector access
Vector access
Vector access
Msync
QN
Vector access
Scalar access
Scalar access
Vector access
Vector access
Msync
Vector access
Memory Interface
E Cache
Accesses
Msync Checking
260
Memory
105
NETWORK
MSP
200
107
201
FIG. 2

FIG. 3

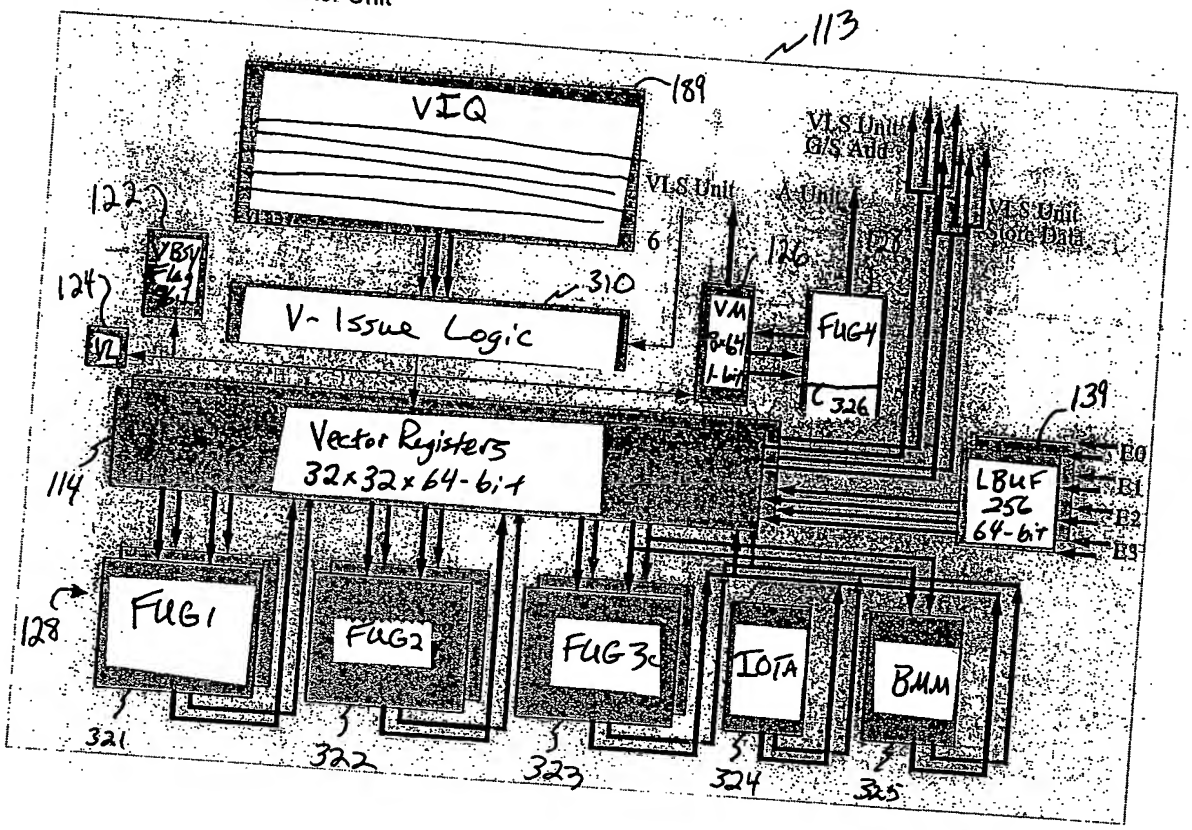
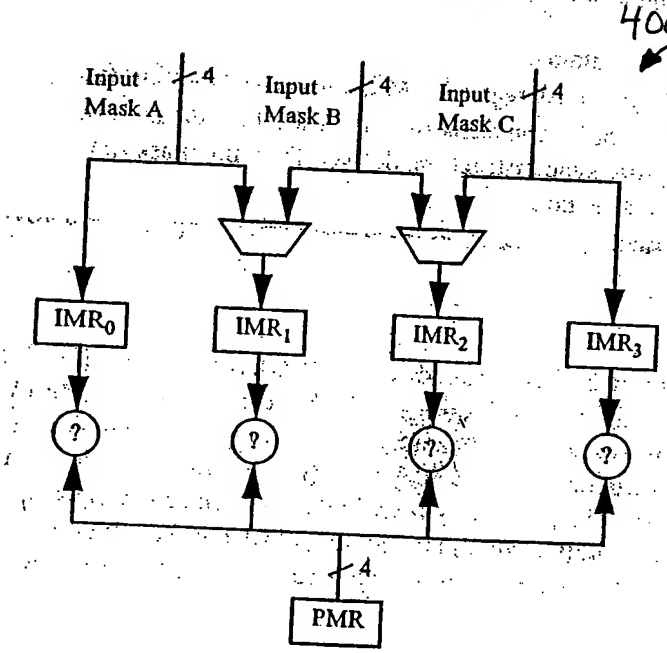


FIG. 4

M/Gsync logic block diagram



Muxing the inputs from the three other processors is controlled by the CPU field of the Config control register.

When there is an executing M/Gsync, a match is detected when all IMRs indicated by the PMR (except the IMR corresponding to the local P chip, which is ignored), match the bit pattern in the PMR. In this case, the Sync completes, and the PMR and participating IMRs are cleared.

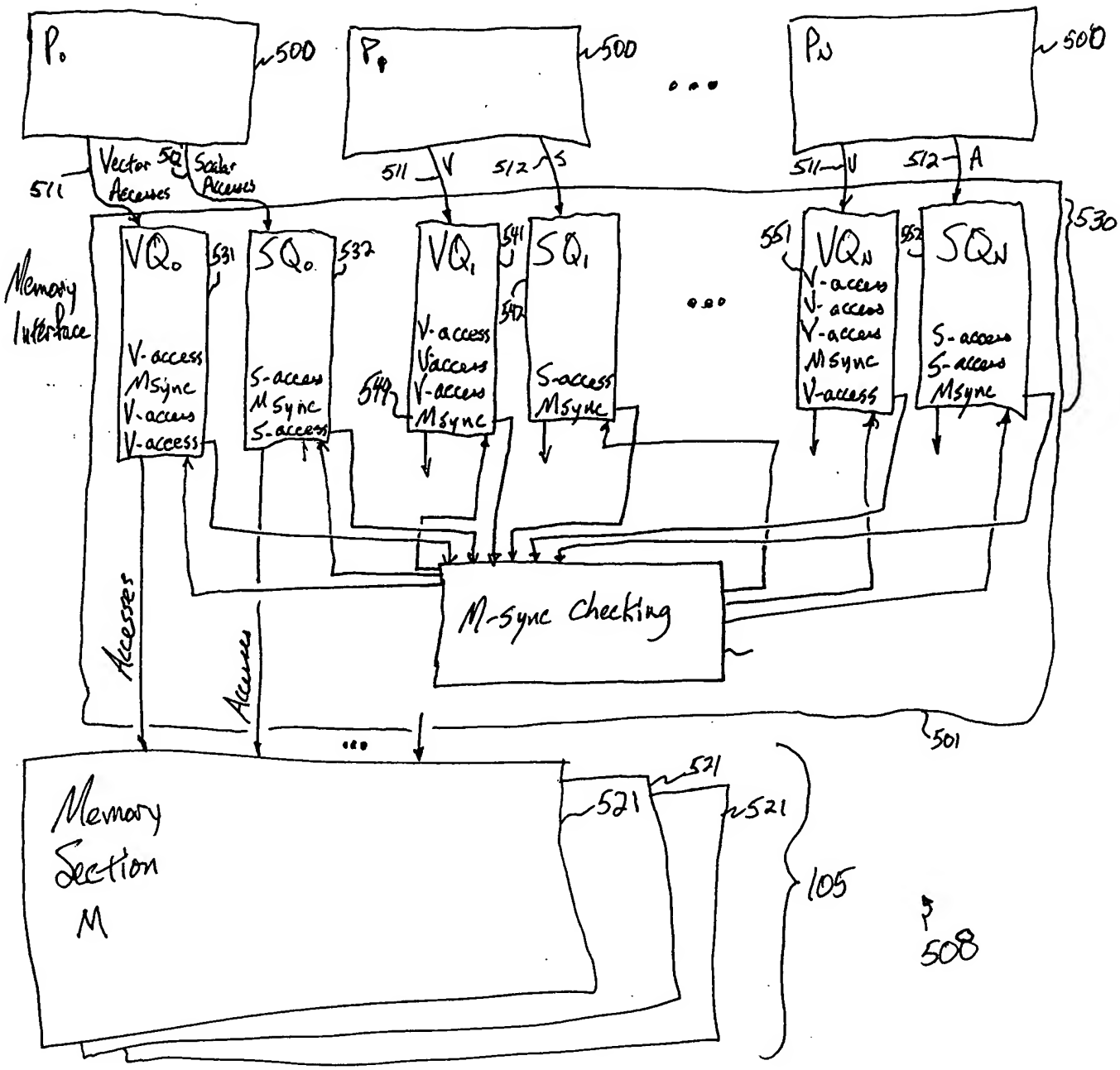

P0
500
P1
500
PN
500
Vector Accesses
Scalar Accesses
511
512
V
S
A
VQ0
531
SQ0
532
VQ1
541
SQ1
542
VQN
551
SQN
552
530
V-access
Msync
S-access
549
M-Sync Checking
Accesses
501
Memory Section M
521
105
508

FIG. 5